ABSTRACT OF THE DISCLOSURE

A buffer circuit includes first to sixth transistors. The first transistor is coupled between a first power source and a first node, and has a gate for receiving a first signal having a first signal level. The second transistor is coupled between the first node and a second power source, and has a gate for receiving a second signal having a second signal level, which is an inverse of the first signal level. The third transistor has a gate coupled to the first node, and is coupled between the first power source and a second node. The fourth transistor is coupled between the second node and the second power source, and has a gate for receiving the first signal. The fifth transistor has a gate coupled to the second node, and is coupled between the first power source and an output end. The sixth transistor has a gate coupled to the first node, and is coupled between the output end and the second power source. In addition, a capacitance is formed between the gate of the sixth transistor and the output end.